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11/16/01

CLAIMS 1-10 CANCELED

CLAIM 11 (NEW)

11. A solid state imaging device comprising:
a two-dimensional array of pixels defining an image plane; and
readout electronics comprising at least one store circuit laterally adjacent the image plane for reading signals therefrom.

CLAIM 12 (NEW)

12. A solid state imaging device according to Claim 11, further comprising a multiconductor signal bus connected between said array of pixels and said readout electronics.

CLAIM 13 (NEW)

13. A solid state imaging device according to Claim 12, wherein each pixel comprises:
a photosensitive diode; and
a switching circuit for resetting and discharging said diode, said switching circuit comprising
a first transistor for applying a reset pulse,
and
a second transistor for connecting said diode to a conductor within said multiconductor signal bus.

CLAIM 14 (NEW)

14. A solid state imaging device according to Claim 11, wherein said multiconductor signal bus comprises a plurality of stacked conductors.

CLAIM 15 (NEW)

15. A solid state imaging device according to Claim 11, wherein said readout electronics are laterally adjacent one side of the image plane.

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CLAIM 16 (NEW)

16. A solid state imaging device according to Claim

11, wherein said readout electronics are laterally adjacent two opposing sides of the image plane.

CLAIM 17 (NEW)

17. A solid state imaging device according to Claim

11, wherein all pixels of said array of pixels are reset

simultaneously and are read out simultaneously.

CLAIM 18 (NEW)

18. A solid state imaging device according to Claim

11, wherein said at least one store circuit comprises a

plurality of store circuits, with a store circuit

corresponding to each pixel and comprising:

a first store circuit for storing a reset value; and

a second store circuit for storing a read out value, with the read out value of a given pixel being modified by the stored reset value for that pixel.

CLAIM 19 (NEW)

19. A solid state imaging device according to Claim

18, wherein each store circuit further comprises:

a third store circuit for storing a second reset value, with a current reset value and a current read out value being processed simultaneously based upon application of a new reset pulse.

CLAIM 20 (NEW)

20. A solid state imaging device according to Claim

19, wherein said readout electronics further comprises:

a differential amplifier connected to said first, second, and third store circuits; and

a reset circuit for placing said differential amplifier in a common mode reset state prior to reading a signal.

CLAIM 21 (NEW)

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21. A solid state imaging device comprising:
a two-dimensional array of pixels defining an image plane, each pixel comprising a photosensitive diode, and a switching circuit for resetting and discharging said diode;
a signal bus connected to said array of pixels; and
readout electronics comprising at least one store circuit laterally adjacent the image plane and connected to said signal bus for reading signals from said array of pixels.

CLAIM 22 (NEW)

22. A solid state imaging device according to Claim 21, wherein said signal bus comprises a multiconductor signal bus; and wherein said switching circuit comprises:
a first transistor for applying a reset pulse; and
a second transistor for connecting said diode to a conductor within said multiconductor signal bus.

CLAIM 23 (NEW)

23. A solid state imaging device according to Claim 21, wherein said signal bus comprises a multiconductor signal bus comprising a plurality of stacked conductors.

CLAIM 24 (NEW)

24. A solid state imaging device according to Claim 21, wherein said readout electronics are laterally adjacent one side of the image plane.

CLAIM 25 (NEW)

25. A solid state imaging device according to Claim 21, wherein said readout electronics are laterally adjacent two opposing sides of the image plane.

CLAIM 26 (NEW)

26. A solid state imaging device according to Claim 21, wherein all pixels of said array of pixels are reset simultaneously and are read out simultaneously.

CLAIM 27 (NEW)

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27. A solid state imaging device according to Claim 21, wherein said at least one store circuit comprises a plurality of store circuits, with a store circuit corresponding to each pixel and comprising:

a first store circuit for storing a reset value; and

a second store circuit for storing a read out value, with the read out value of a given pixel being modified by the stored reset value for that pixel.

CLAIM 28 (NEW)

28. A solid state imaging device according to Claim 27, wherein each store circuit further comprises:

a third store circuit for storing a second reset value, with a current reset value and a current read out value being processed simultaneously based upon application of a new reset pulse.

CLAIM 29 (NEW)

29. A solid state imaging device according to Claim 28, wherein said readout electronics further comprises:

a differential amplifier connected to said first, second and third store circuits; and

a reset circuit for placing said differential amplifier in a common mode reset state prior to reading a signal.

CLAIM 30 (NEW)

30. A method for making a solid state imaging device comprising:

defining an image plane using a two-dimensional array of pixels; and

placing readout electronics laterally adjacent the image plane for reading signals from the array of pixels, the readout electronics comprising at least one store circuit.

CLAIM 31 (NEW)

31. A method according to Claim 30, further comprising connecting a multiconductor signal bus between the array of pixels and the readout electronics.

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CLAIM 32 (NEW)

32. A method according to Claim 30, further comprising forming each pixel using a photosensitive diode, and a switching circuit connected thereto for resetting and discharging the diode.

CLAIM 33 (NEW)

33. A method according to Claim 32, wherein the switching circuit comprises a first transistor for applying a reset pulse, and a second transistor for connecting the diode to a conductor within the multiconductor signal bus.

CLAIM 34 (NEW)

34. A method according to Claim 30, wherein the multiconductor signal bus comprises a plurality of stacked conductors.

CLAIM 35 (NEW)

35. A method according to Claim 30, wherein the readout electronics are placed laterally adjacent one side of the image plane.

CLAIM 36 (NEW)

36. A method according to Claim 30, wherein the readout electronics are placed laterally adjacent two opposing sides of the image plane.

CLAIM 37 (NEW)

37. A method according to Claim 30, wherein the image device is configured so that all pixels of the array of pixels are reset simultaneously and are read out

CLAIM 38 (NEW)

38. A method according to Claim 30, wherein the at least one store circuit comprises a plurality of store circuits, with a store circuit corresponding to each pixel and comprising a first store circuit for storing a reset value, and a second store circuit for storing a read out value, with the read out value of a given pixel being modified by the stored reset value for that pixel.

CLAIM 39 (NEW)

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39. A method according to Claim 38, wherein each store circuit further comprises a third store circuit for storing a second reset value, with a current reset value and a current read out value being processed simultaneously based upon application of a new reset pulse.

CLAIM 40 (NEW)

40. A method according to Claim 39, further comprising:

connecting a differential amplifier to the first, second and third store circuits; and

connecting a reset circuit to the differential amplifier for placing the differential amplifier in a common mode reset state prior to reading out a signal.